

Physical Design Guidelines

This document describes the recommendations for hand-off of gate level netlist designs to the physical design processes at Qthink.

The recommendations are divided into **Rules, Suggestions and Good Design Practices**.

Rules must be followed for the hand-off. Most of these can be checked automatically when the design is initially input into the physical design tools.

Suggestions would be useful for either making the design easier to meet the various design objectives, such as die size, performance, power, etc, or for ease of understanding.

Good Design Practices will help avoid mistakes that are easy to overlook and that make the design more robust, or that aid in ease of understanding.

Netlist:

Most of these rules are mandated by EDA tools and the Verilog language definition which assume certain conventions for the signal/port/module names.

Rules :

- ❑ The netlist should be released in the verilog netlist format.
- ❑ There should not be any assign statements in the verilog netlist.
- ❑ Names must use extended alphanumeric set [A..Za..z0..9_] only and they must start with a letter. They cannot start or end with "_" and should not contain two consecutive "__".
- ❑ No bus signal should be used as a clock.
- ❑ The same name should be used across hierarchy for clocks driven from the same source.
- ❑ Do not use case sensitivity to distinguish between names.

Suggestions :

- ❖ No vectors should contain a digit at the end of the name (e.g. ram_addr2[7:0]).

Good Design Practice:

- One statement per line
- One port declaration per line.
- Use a simple and consistent naming convention.
e.g.

| Suffix/Prefix | Signal Functionality |
|---------------|----------------------|
| _a | Asynchronous Signal |

| | |
|-------|----------------------------------|
| _z | Tri-state Signal |
| _p | Open drain outputs and Pull-ups |
| _r | Registered Outputs |
| 1d/2d | Pipelined signals |
| _n | Active Low Signals |
| _v | Analog Voltage Signal |
| _I | Analog Current Signal |
| _q | Intentionally Latched Signal |
| _nc | Intentionally Unconnected Signal |
| Clk_ | Clock Signal |
| Rst_ | Reset Signal |

- Lower case signal and port names are preferred.
- Names should preferably be less than 25-30 characters long.
- All clocks should contain the string "clk" in their names (helpful for scripting).
- Signals assigned from the reset port should contain the string "rst" in their names.
- Port declarations should be sorted by type and then by functionality.
e.g.
Inputs:
Reset
Clocks
Control Signals
Datapath Signals

Outputs:
Reset
Clocks
Control Signals
Datapath Signals

Inouts:
Control Signals
Datapath Signals

Inouts should be used only at the top-level.
- Use a standard header for all files containing: Author, Date of Creation, Version Control information, Copyright Notice and Functional/Interface description with timing diagram if appropriate.

Timing Constraints:

Rules:

- ❑ The constraints must be such that they can be applied in one sequence, and from which a single, accurate timing report can be generated with no false errors.
- ❑ The supplied constraints must be the set for which final signoff for timing will occur.

- ❑ The pre-layout wire load model-based synthesis must be performed with at least a 10% positive timing margin.
- ❑ For each clock, whether externally or internally generated, the constraints must include settings for clock period, rise/fall times, and targets for insertion delay, skew and transition times.
- ❑ For each input pin, the constraints must include settings for arrival time and a driving cell (or resistance).
- ❑ For each output pin, the constraints must include settings for departure time and output load.
- ❑ The constraints must include all false paths and multi-cycle paths in the design.
- ❑ The constraints must include settings for wire load models.
- ❑ The constraints must include settings for process, voltage and temperature (PVT).
- ❑ A dump file of the top 100 critical nets in the design must be provided, to be used for timing correlation of the physical layout tool's static timing analysis engine.
- ❑ If specific requirements for maximum transition times on signals are required, which are tighter than what is listed in the .lib file, these must be specified at the time the netlist is delivered.

Suggestions :

- ❖ The timing constraints should be in Synopsys SDC format. If another format is to be supplied, please check first with QThink for compatibility with our physical design processes.
- ❖ Fanouts greater than 16 should be avoided in all cases except for special signals such as clocks, scan enables, and reset signals. Any high fanout signals that remain in the netlist must be identified, and their functional purpose described.
- ❖ If scan is included in the design, a separate set of constraints may be needed to verify hold time checks during the scan operation.
- ❖ The constraints should only reference leaf cell pins, not the pins of intermediate hierarchical modules.
- ❖ Provide proper synchronization at the system level for signals crossing clock domains or for asynchronous inputs, such that these signals can be included as false paths in the constraints.
- ❖ Provide circuit diagrams and timing diagrams showing the relationships between all the clock domains, and their interaction with the PLL (if any).
- ❖ Spare logic gates that are added into the netlist by the customer should have the inputs tied low. Spare FFs that are added should have their clock, reset and scan pins connected to a signal of the appropriate type. There should be at least one spare gates module for each physical block.
- ❖ The pre-layout wire load model-based synthesis should be performed with at least a 20% positive timing margin.

Good Design Practice :

- The constraints script should use relative pathnames for directories.
- Library, technology and environment should be parameterized inside the script.

Physical Partitioning:

Rules:

- ❑ For full chip designs, the netlist must contain the I/Os
- ❑ The cell utilization in the standard cell rows must be less than 80%.

Suggestions :

- ❖ Limit the number of physical blocks to less than 20 at any level in the hierarchy, to minimize complexity.
- ❖ All physical block inputs and outputs should be registered. This simplifies meeting the timing constraints at the top level.
- ❖ Minimize physical block interface signals.
- ❖ Avoid "feed-through" signals or snake paths (signals that traverse many physical block boundaries).
- ❖ Physical blocks should be of reasonable size, with 100K instances as a typical number, and 300K as the upper limit. This will help insure manageable run times for timing-driven tools.
- ❖ The cell utilization in the standard cell rows should be in the range of 60% – 70%.

Good Design Practice :

- No glue logic at the top level.
- Partition random logic separate from structured logic so they can be individually place/routed, if necessary.

Physical Verification:

Rules:

- ❑ There should only be one DRC, LVS and antenna deck to be used for physical verification.
- ❑ All the cells in the library, including standard cells, memories, custom digital and analog blocks, must be clean through the single DRC and LVS decks.